IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Lee D. Whetsel**

Serial No: **TBD** 10/618920

Filed: **Herewith**

Attorney Docket No. **TI-30102.1**

Group: **TBD**

Examiner: **TBD**

Correctly

For: **QUAD STATE LOGIC DESIGN METHODS, CIRCUITS, AND SYSTEM**

PRELIMINARY AMENDMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Please amend the above-referenced application as follows:

IN THE SPECIFICATION:

Page 1, after the title, insert the following added paragraph, --This is a divisional application of Serial No. 09/767,318 filed 01/22/2001, which is now a U.S. Patent 6,636,076 which claims priority under 35 USC 119(e)(1) of provisional application Serial No. 60/171,039, filed 12/16/1999--.

IN THE CLAIMS:

Claims 1-17 (cancelled)

Claim 18 (new) A memory for storing any one of four voltage level inputs comprising;

an input for receiving said voltage level inputs,

storage circuitry for latching said voltage level inputs,

circuitry for performing a Boolean logic operation on said latched voltage levels and;

an output for transmitting a signal indicative of said Boolean logic operation performed on said latched voltage levels.